Claim 1 – Art Rejection Under Section 103(a)

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Burr in view of Yamaguchi and/or K '470. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that "the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via said contact portion for the first transistor and a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state; and wherein the first MOS transistor comprise a P-type well and the second MOS transistor comprises a N-type well formed in the semiconductor substrate, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other." The cited art fails to disclose or suggest these aspects of claim 1 for at least the following reasons.

First, claim 1 requires that the impurity diffusion layer and the S/D regions be of *different* conductivity types, and that the contact hole reaches the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer, and wherein the conductor in the contact hole is electrically isolated from the semiconductor layer by at least the device isolation region. The Office Action admits that Burr fails to disclose or suggest these aspects of claim 1, and thus cites to KR '470.

The Section 103(a) combination of Burr and KR '470 is fundamentally flawed and legally incorrect.

Burr discloses a diffusion layer (e.g., well 750) and source/drain regions (e.g., 712, 714) of *different* conductivity types. As admitted in the Office Action, Burr does not describe or suggest a potential applied from above the substrate via an isolation region which is switched between the standby and operative states as required in claim 1. However, given these different conductivity types, Burr repeatedly states that the diffusion layer must be aligned directly under only the intrinsic channel region (i.e., diffusion layer ***cannot*** extend outside of the S/D regions, and thus cannot receive the contact as claimed here) (e.g., col. 5, lines 54-56; col. 7, lines 18-20). Thus, Burr requires a well contact from the substrate side (not the transistor side) which is directly contrary to the invention of claim 1.

Recognizing that Burr fails to disclose or suggest the diffusion layer contact arrangement required by claim 1, the Office Action cites to KR '470. KR '470 discloses an expanded back gate which extends past the channel and source/drain regions so that a contact can be made from the transistor side of the substrate. KR '470 has an N-well and P-well which contact each other-directly contrary to what claim 1 requires. Moreover, the only reason that KR '470 can extend its back gate 20, 24 past the channel and source/drain regions to enable contact is because the back gate is always of the *same* conductivity type as the source/drain (opposite of Burr). When KR '470 is applied to an n-type MOSFET, both the back gate and source/drain regions are apparently n-type, and

when applied to a p-type MOSFET both the back gate and the source/drain regions are p-type. In KR '470, since the back gate and source/drain regions have the same conductivity type, the back gate can be expanded without adversely affecting transistor operation.

However, there is no suggestion in the art of record that would have caused one of ordinary skill in the art to have expanded a diffusion layer as required by claim 1 so as to be located under at least the channel and source/drain regions in a situation where the diffusion layer is of a *different* conductivity type than the source/drain regions as required by claim 1. In contrast, Burr teaches that this should not be done. KR '470 also teaches directly away from the invention of claim 1 since KR requires that the adjacent P and N wells of adjacent different transistors contact each other. The invention of claim 1, by having the N-well and P-well formed via the substrate, can alleviate contact resistance between the wells and/or increase the parasitic capacitance between the wells, thereby allowing the latch-up resistance to be improved. Accordingly, the Section 103(a) combination of Burr and KR '470 is fundamentally flawed and incorrect.

Second, none of the cited references disclose or suggest that active regions of both transistors are substantially *completely depleted simultaneously in the standby state*.

Third, Burr relates to an entirely different type of device than does KR '470. Burr's adjacent transistors 702 and 704 are electrically isolated from one another via "Ox" provided therebetween. Since the overall transistors 702 and 704 are electrically isolated in Burr, it makes sense to also electrically isolate the two wells located beneath the

respective transistors. However, in clear contrast with Burr, adjacent transistors in KR '470 are not electrically isolated from one another. Instead, they share the same semiconductor material and the alleged back gates are immediately adjacent. In other words, KR '470 and Burr utilize opposite types of structure. Thus, one of ordinary skill in the art would not have made the alleged combination of opposite types of structure as alleged in the Office Action.

Claim 7

Claim 7 requires that "the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via said contact portion for the first transistor and a separate contact region including a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state; and wherein the first MOS transistor comprise a P-type well and the second MOS transistor comprises a N-type well formed in the semiconductor substrate, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other." The cited art fails to disclose or suggest these aspects of claim 7.

Claim 24

Claim 24 requires "a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being substantially isolated from one another; and respective contact portions for

applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are substantially completely depleted simultaneously in the standby state, wherein said contact portions are electrically insulated from said semiconductor layer." Again, the cited art fails to disclose or suggest these aspects of claim 24.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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